

5   **WHAT IS CLAIMED IS:**

1.           A desynchronizer for desynchronizing a plurality of data channels of SONET/SDH data signals, comprising:

10           (a) a plurality of first in first out buffer (FIFO) blocks, one for each of said data channels, said FIFO blocks each having respective FIFO read and write address outputs, a gapped clock input operative in response to gapped clock signals, to store input data extracted from a SONET/SDH frame;

15           (b) an arithmetic unit having a phase word output and inputs coupled to the read and write address outputs of each of said FIFO blocks, operative to calculate an address difference of the read and write addresses for each of said FIFO blocks and a  
20           phase locked loop (PLL) phase increment value, which depends on the address difference and a pointer adjustment phase difference and adding or subtracting a small number to provide a total phase increment from said phase word output for each of said FIFO blocks;

25           (c) an endless phase modulator common control block coupled to an output of said arithmetic unit operative to produce delay tap selection signals in response to corresponding total phase increment signals from said arithmetic control unit;

30           (d) an oscillator; and

(e) an endless phase modulator coupled to an output of said endless phase modulator common control block and to said oscillator and operative in response to said delay tap selection signals to generate clock signals frequency shifted from said oscillator clock frequency and to apply said clock signals to respective desynchronized clock inputs of said FIFO buffer blocks and to thereby clock out desynchronized data signals from said FIFO buffer blocks.

15 2. The desynchronizer according to claim 1, wherein said endless phase modulator includes a delay line having delay elements with taps at junctions of said delay elements and a plurality of modulator multiplexers, one for each of said plurality of data channels, coupled to said taps and operative to  
20 select a delay tap selection signal in response to receipt of a tap select signal.

3. The desynchronizer according to claim 2, wherein the delay elements are buffers.

4. The desynchronizer according to claim 2, wherein each of said delay tap selection signals is provided with a plurality of independent outputs, one corresponding to each of said data channels, with outputs of said taps coupled to inputs of  
30 corresponding ones of said modulator multiplexers.

5 5. The desynchronizer according to claim 2, including a calibration circuit having a pair of calibration multiplexers whose inputs are coupled to said delay tap selection signals and are operative to output a selected delay tap selection signal in response to a select tap number signal from said endless phase  
10 modulator.

6. The desynchronizer according to claim 1, wherein said arithmetic unit includes a write multiplexer and a read  
15 multiplexer having inputs coupled to respective write and read address outputs of said FIFO blocks and an add-subtract circuit having a first input coupled to an output of said write multiplexer and a second input coupled to an output of said read multiplexer, a register that latches an output of said add-subtract circuit and RAM storage for storing information used in  
20 calculating a phase increment for each channel.

7. The desynchronizer according to claim 6, wherein said RAM storage includes two RAM blocks with an output of a first of said two RAM blocks coupled to an input of said write multiplexer  
25 and an output of said second of said two RAM blocks coupled through a third multiplexer to an input of said second multiplexer and an input of a control circuit and wherein said control circuit controls operation of said two RAM blocks, said read and write multiplexer, said register, said third multiplexer  
30 and said add-subtract circuit.

5 8. The desynchronizer according to claim 7, wherein said  
third multiplexer scales an accumulated FIFO address difference.

9. The desynchronizer according to claim 5, wherein said  
calibration circuit has logic circuitry which latches a tap  
10 selection signal corresponding to a tap whose delay is one less  
than a tap number whose corresponding delay is the first of an  
increasing sequence of tap numbers to exceed one clock cycle.

10. The desynchronizer according to claim 9, wherein said  
15 arithmetic unit calculates the total phase increment for each of  
the channels in round robin fashion.

11. The desynchronizer according to claim 2, wherein tap  
signals applied to inputs of each modulator multiplexer are  
20 selected on a round robin basis.

12. The desynchronizer according to claim 5, wherein said  
calibration circuit includes a counter to provide tap selection  
signals to said calibration multiplexers and logic circuitry  
25 which causes latching of a tap number from said counter in  
response to a clock signal generated by said logic circuitry.

13. The desynchronizer according to claim 1, including a  
reprogrammable Look-up-Table (LUT) in said endless phase  
30 modulator control circuit operative to convert phase to a tap  
selection signal for application to said channel multiplexers.

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14. The desynchronizer according to claim 1, wherein said arithmetic unit has a read FIFO address arithmetic multiplexer and a write FIFO address arithmetic multiplexer for receiving and storing FIFO read and write addresses from said FIFO read and  
10 write address outputs, an add-subtract circuit coupled to said arithmetic multiplexers operative to add or subtract outputs from said arithmetic multiplexers, a register coupled to an output of said add-subtract circuit, a pair of memory blocks coupled to an output of said register, a current memory block for storing a  
15 current FIFO address and an accumulated memory block for storing an accumulated FIFO address difference, a feedback multiplexer circuit coupled between said another memory circuit and an input to said read FIFO address arithmetic multiplexer, and a control circuit coupled to an output of said feedback multiplexer and  
20 operative to control operation of said arithmetic unit.

15. A method of desynchronizing a plurality of data channels of SONET/SDH data signals, comprising:

25 (a) clocking data receiving data from a SONET/SDH channel in a first-in-first-out buffer (FIFO) using a gapped clock corresponding to data in which overhead has been removed;

(b) calculating a difference between a write address  
30 of said FIFO and a read address thereof and storing a difference in a first memory block;

(c) adding or subtracting a pointer adjustment for a given channel from the difference in step (b);

(d) calculating a phase locked loop increment value  
10 from the difference;

(e) providing extra phase modulation of the output clock so as to leak bits stored in said FIFO related to the pointer adjustment and reduce bandwidth of jitter;

15 (f) adding or subtracting the amount of external phase increment used to extra modulate an endless phase modulator;

(g) generating a tap selection number from said phase  
20 increment and applying said tap selection number to a multiplexer of an endless phase modulator to gate a selected tap signal through said endless phase modulator multiplexer;

(h) applying the selected tap signal to a calibration  
25 circuit to latch a tap number,  $M$ , that is one less than a tap number that corresponds to a delay of one clock cycle;

(i) accumulating the latched tap number  $2N$  times in an arithmetic unit, where  $N$  is an integer, and storing numbers  $2N \times$   
30  $M$  in address locations of a memory block corresponding to each accumulation; and

(j) applying in succession tap select signals increasing from a first tap up to an Mth tap to said channel multiplexer selection inputs so as to reduce the frequency of clock signals passing through said channel multiplexer.

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16. A desynchronizer for desynchronizing a plurality of data channels of SONET/SDH data signals, comprising:

15 (a) a plurality of first in first out buffer (FIFO) blocks, one for each of said data channels, said FIFO blocks each having respective FIFO read and write address outputs, a gapped clock input operative in response to gapped clock signals, to store input data extracted from a SONET/SDH frame;

20 (b) an arithmetic unit having a phase word output and inputs coupled to the read and write address outputs of each of said FIFO blocks, operative to calculate an address difference of the read and write addresses for each of said FIFO blocks and a phase locked loop (PLL) phase increment value, which depends on  
25 the address difference, adding or subtracting a small number to provide a total phase increment from said phase word output;

(c) a numerically controlled oscillator coupled to an output of said arithmetic unit operative to produce a digital  
30 oscillator output;

5 (d) an I and Q signal digital-to-analog converter  
coupled to the output of said numerically controlled oscillator  
and having an analog output;

(e) a crystal oscillator; and

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(f) a single side band modulator coupled to an output  
of said crystal oscillator and to said analog output, operative  
to produce desynchronized clocks coupled to respective FIFO  
channel blocks for clocking desynchronized data signals from said  
15 FIFOs.

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17. A multiple channel desynchronizer for desynchronizing a  
plurality of data channels, comprising:

20 a single desynchronizer operative to desynchronize data  
from each of said channels in turn.

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18. A method of desynchronizing data signals on a plurality  
of channels of SONET/SDH signals, comprising:

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(a) storing data, extracted from SONET/SDH frames on  
said plurality of channels, in a FIFO block using a gapped  
clocks;

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(b) calculating an address difference between write  
and read addresses of each of said FIFO blocks and a phase locked



5 loop total phase increment value which depends on said address  
difference;

(c) producing a delay tap control signal for each  
channel from said total phase increment value for selecting a  
10 delay of an oscillator signal from said oscillator for said each  
channel; and

(d) producing desynchronized clock signals from said  
delayed oscillator signals and applying said clock signals to  
15 clock out desynchronized data from said FIFO's.